35 GHz GaAs Power MESFET's and Monolithic Amplifiers

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Abstract—**GaAs MESFET's have been optimized for power operation at 35 GHz. Various doping levels and potential barrier layers at the interface between the buffer and the active layer have been studied. The best power performance has been obtained from the FET on a very heavily doped active layer [1]. The device on AlGaAs heterobuffer had further improved output power. The best devices delivered output power densities of 0.8 W/mm with 23 percent efficiency, 0.71 W/mm with 34 percent efficiency, and 0.61 W/mm with 41 percent efficiency. Monolithic power amplifiers with a 400 μm FET have generated 200 mW of output power. These amplifiers were monolithically power combined, resulting in 600 mW of output power at 34 GHz.**

I. Introduction

IMPROVED techniques for processing a sub-half-micrometer-gate FET and GaAs epi-layer formation have made it possible to optimize the GaAs power FET's at millimeter-wave frequencies [2]–[4]. Due to short gate length, the active layer needs to be thin to overcome the short-channel effect. Consequently, a highly doped channel layer [1], [5] is generally used to allow for the high current-handling capability required for power generation. The best performance at 35 GHz has been obtained from a MESFET on upper $\times 10^{17}$ cm^{-3} doped active layer [1]. Although the doping level was high, the gate-to-drain breakdown voltage of the FET remained high, operating at about 6 V at the drain. The reason is the nonuniform field distribution under the gate [6]. However, MESFET's tend to operate better at slightly lower drain bias voltages as the doping level increases. Therefore, the output power per unit gate width decreases as the operating frequency increases [4]. The short-channel effects could be further reduced by using a barrier layer at the interface between the active layer and the buffer. The barrier is formed using either a p^+ layer at the interface [7], [8] or an AlGaAs heterobuffer layer [9], [10].

Monolithic power amplifiers at 35 GHz have been developed. The circuit of the amplifier reported in [4] has been improved further to have power matching at the 32 to 34 GHz band. These amplifiers were power-combined in a single chip. The resulting device delivered 600 mW of output power at 34 GHz [11]. The monolithic implementation of matching circuits is even more advantageous at millimeter-wave frequencies than at microwave frequencies, because the matching circuits are very small and it is easier to place the precise components required at high frequencies in monolithic forms than in the hybrid forms [12]. In this paper, we describe the power performance of various MESFET's and monolithic amplifiers.

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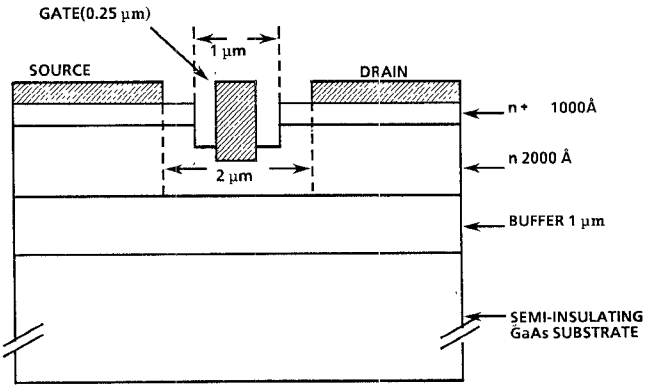

Fig. 1. An n^+ ledge channel structure MESFET with a 0.25 μm gate.

II. MESFET Optimization

The n^+ ledge channel structure (or "double recess channel structure") MESFET shown in Fig. 1 has been optimized as a power device at 35 GHz. It has been shown that devices with this structure have the highest resistance to instantaneous burnout and the highest long-term reliability [13]. The n^+ ledge structure also significantly improves device microwave performance over that of conventional recessed gate devices [14]. The performance improvement is attributed to the reduced parasitic resistance of the source–gate and drain–gate regions and the shallower gate recess allowed for this structure, thereby reducing parasitic capacitances [15].

The required material was grown by molecular beam epitaxy (MBE). MBE presents several advantages that no other material preparation technique can offer. First, the abrupt transition at the active layer–buffer interface can

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be produced. Second, multilayer structures with precise control of the layer thicknesses required for AlGaAs buffer or p^+ buffer MESFET's can be grown. A highly doped n^+ layer can also be grown. More importantly, the quality of the material may be superior to that of the ion-implanted material or VPE material.

Power operation requires a MESFET with a small-signal gain of more than 8 dB, and high efficiency calls for a power gain of at least 5 dB. To achieve the high gain, sub-half-micrometer-gate MESFET's have been fabricated. A typical 0.2-μm-gate MESFET (see Fig. 1) has been proposed on a standard (mid$\times 10^{17}$ cm^{-3}) doped active layer without any barrier [4]. The best result we have achieved from this structure is a 33 percent power-added efficiency with a power density of 0.53 W/mm at 35 GHz. To further improve the power performance, we have investigated three structures for reducing the short channel effects: (1) a p^+ barrier layer, (2) an AlGaAs heterobuffer, and (3) a very heavily doped active layer. For the first attempt, a p^+ barrier layer with a partial depletion has been grown under the standard doped active layer, and 0.35 μm gate FET's have been processed on this material and RF tested. The FET's had transconductances of 400 mmho/mm and small-signal gains of 8 dB at 54 GHz. This gain is high compared with conventional MESFET's. However, when the drain was biased more than 5 V, a parasitic bipolar action occurred [7], indicating that the p^+ layer was not completely depleted. When the bipolar mode of operation occurred, the device gain dropped to an unacceptable range, and the device could not operate properly at a high power level. Another MBE slice with a thinner p^+ layer with complete depletion has been grown, and 0.2-μm-gate MESFET's have been produced. The dc characteristics of the device are shown in Fig. 2. The transconductance was 200 mmho/mm. The output conductance was very small, as seen from the drain current in the saturation region, which was almost constant with increasing drain voltage. The p^+ layer was completely depleted, and we saw no parasitic bipolar action. At 35 GHz, a small-signal gain of 13.5 dB was achieved. When tuned for power, the device was capable of 0.42 W/mm power density with 4 dB gain (the corresponding linear gain was 6.5 dB). The small-signal gain of the FET on the p^+ barrier was apparently very high, but the power performance was rather poor.

Another way of generating a barrier layer is to use an AlGaAs heterobuffer. We have grown a $Al_{0.4}Ga_{0.6}As$ heterobuffer epi-layer by using MBE. The active layer doping was upper$\times 10^{17}$ cm^{-3}. FET's with 0.25 μm gates have been produced on this material and tested. Fig. 3 shows the dc characteristics of a 0.25 μm$\times$75 μm MESFET. The saturation current density was 373 mA/mm, the maximum current density (with +1 V at the gate) was 560 mA/mm, and the gate–drain breakdown voltage was 12 V. Maximum transconductance was 250 mmho/mm. At 35 GHz, a small-signal gain of 11.5 dB was achieved. When tuned for power, the device gave a power density of 0.8 W/mm with 4 dB gain and 23 percent efficiency (the corresponding linear gain was 6.5 dB). A maximum efficiency of 30 percent was obtained with a power density of 0.52 W/mm and 5.4 dB gain. The power performance of the MESFET on AlGaAs buffer was very good, but the power gain and efficiency were a little low because of the lower transconductance (about 15 percent lower than the comparable standard MESFET's).

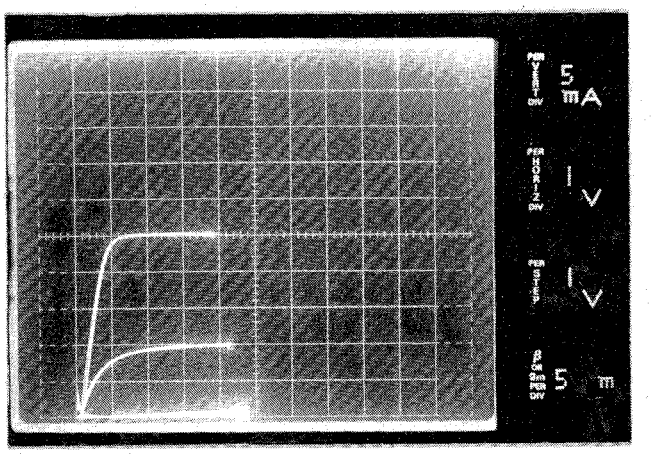
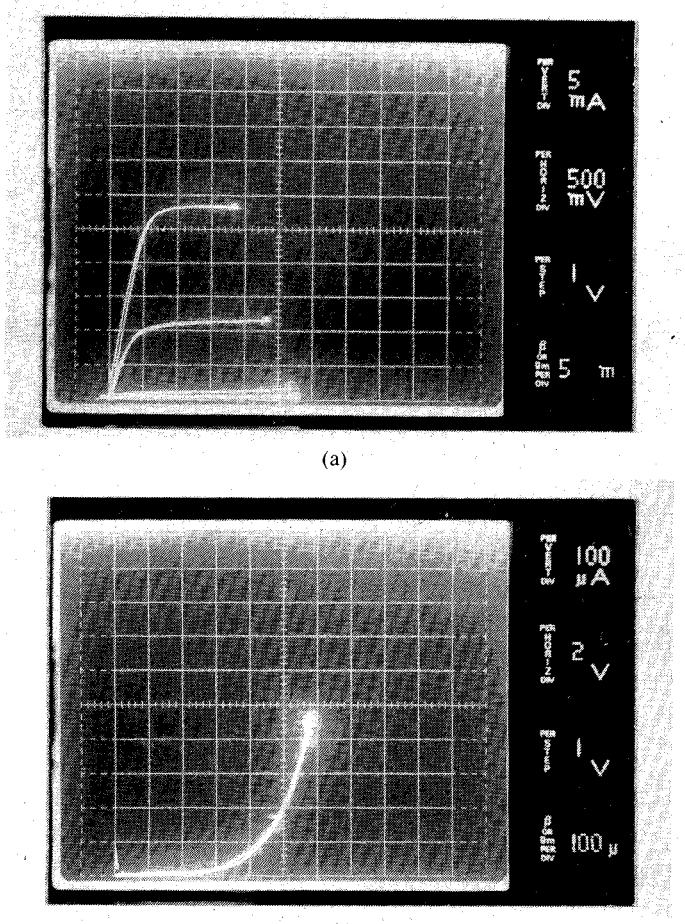


Fig. 2. I–V characteristics of a 0.2$\times$75 μm^2 MESFET with p^+ barrier layer.

A 0.2 μm$\times$75 μm MESFET was built on a very heavily doped active layer (doping level of upper $\times 10^{17}$cm^{-3}) and RF tested [1]. We obtained a power density of 0.71 W/mm with a power-added efficiency of 34 percent and 5.2 dB power gain. When the device was tuned for maximum efficiency at a slightly reduced drain bias, we obtained a power-added efficiency of 41 percent with a power density of 0.61 W/mm and 5.6 dB gain (see Fig. 4). This is the best performance ever achieved with a GaAs MESFET at this frequency. The most significant result is the simultaneous achievement of high values of power density, efficiency, and gain. The results are attributed to the use of the very thin active layer, which reduces short-channel effects while maintaining the relatively high breakdown voltages.

The power performance results for the various FET's are summarized in Table I. The data have clearly shown that a very heavily doped active layer is needed for a power MESFET at millimeter-wave frequencies, and use of a heavily doped layer does not degrade the device breakdown voltage significantly. The AlGaAs buffer layer enhanced the power density somewhat, but the power gain was lower than that of a standard MESFET. The p^+ barrier layer improved the small-signal gain, but the power performance was rather poor. The power densities of the MESFET's may be related to the active layer charge distribution profiles. As shown in Fig. 5, the charge is depleted at the p^+ and active layer interface, while it is confined tightly at the heterointerface. Although the performance of these devices is already very good, further improvements are expected by further optimizing the device structures, such as the doping level and thickness of the active layer and the Al content of the AlGaAs buffer layer.



(a)

(b)

Fig. 3. The dc characteristics of a 0.25×75 μm^2 MESFET with $Al_{0.4}Ga_{0.6}As$ buffer. (a) $I-V$ curve. (b) Gate–drain breakdown curve.

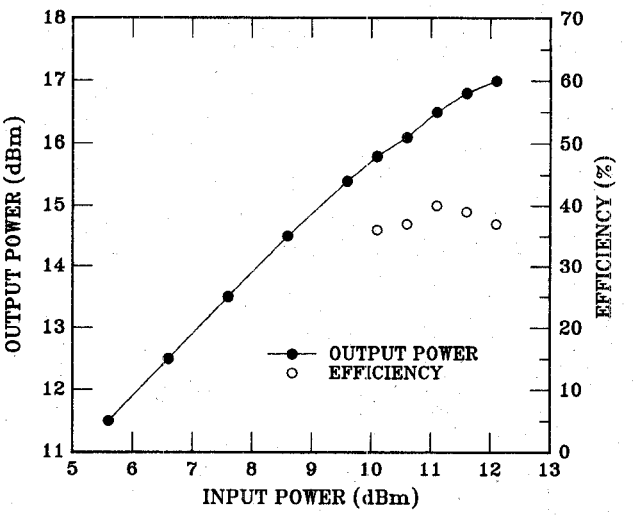


Fig. 4. Gain compression characteristic of a 0.2 $\mu m \times 75$ μm MESFET on a heavily doped layer.

TABLE I
POWER PERFORMANCE OF MESFET'S AT 35 GHz

	Power Density W/mm	Power Gain (dB)	Efficiency (%)
Standard MESFET	0.53	4.7	33
MSEFET on Heavily Doped Layer	0.61	5.6	41
MESFET with AlGaAs Buffer	0.8	4	23
MESFET with p + Barrier Layer	0.42	4	18

III. Amplifier Design and Fabrication

At millimeter-wave frequencies, impedance matching of the active device needs to be treated at the time the device configuration is designed. Any parasitics must either be minimized or taken into consideration in the amplifier design. Fig. 6 shows the circuit topology of a 35 GHz amplifier. This amplifier consists of two 200-μm-gate-width FET cells reactively combined on-chip. The optimized circuit element values were obtained by a conventional computer optimization technique using FET models generated from S-parameter measurements. A characteristic impedance of 75 Ω was used for the transmission lines. This circuit is power-matched at around the 32 to 34 GHz band. Fig. 7 shows the completed amplifiers that have the circuit topology shown in Fig. 6. The chip sizes are $21 \times 21 \times 4$ mils.

Following epitaxial layer growth, AuGe/Ni/Au ohmic contacts were formed. For device isolation, boron implantation was used instead of mesa etching to avoid crossing a mesa step with a very narrow gate. The wide recess pattern of the n^+ ledge structure was then defined in PMMA by electron beam lithography, and the channel was etched through the n^+ layer into the n layer. The gate pattern was then similarly defined in a PMMA layer, and the GaAs was etched again down to the final desired saturation current value. The Ti/Pt/Au gates were then fabricated. The same set of alignment marks were used for both the wide recess and the gate definition. An Au layer a few micrometers thick was then evaporated and lifted off to produce the capacitor bottom plates, inductors, and source grounding pads. MIM capacitors with a Si_3N_4 dielectric layer were fabricated, followed by plated gold air bridges for contacting FET sources and capacitor top plates. Transmission lines and all pads were also plated with gold at the same time. The slice was then lapped to a thickness of 100 μm. Grounding vias (2×3 mils) were etched by the reactive ion etching technique. A plated gold heat sink interconnects all the vias.

The power saturation characteristics of these amplifiers (based on a 0.25 μm MESFET processed on a standard doped epi-layer) were tested. As designed, the small-signal gain of the 400 μm FET amplifier was about 7 to 8 dB across the 30 to 34 GHz band. The best amplifier generated 200 mW of output power (0.5 W/mm) with 3.8 dB gain and 21 percent power-added efficiency at 34 GHz [4]. The 1 dB gain compression output power was 170 mW with 5 dB gain and 23 percent power-added efficiency. The drain and gate biases were 7.1 V and -1.6 V, respectively.

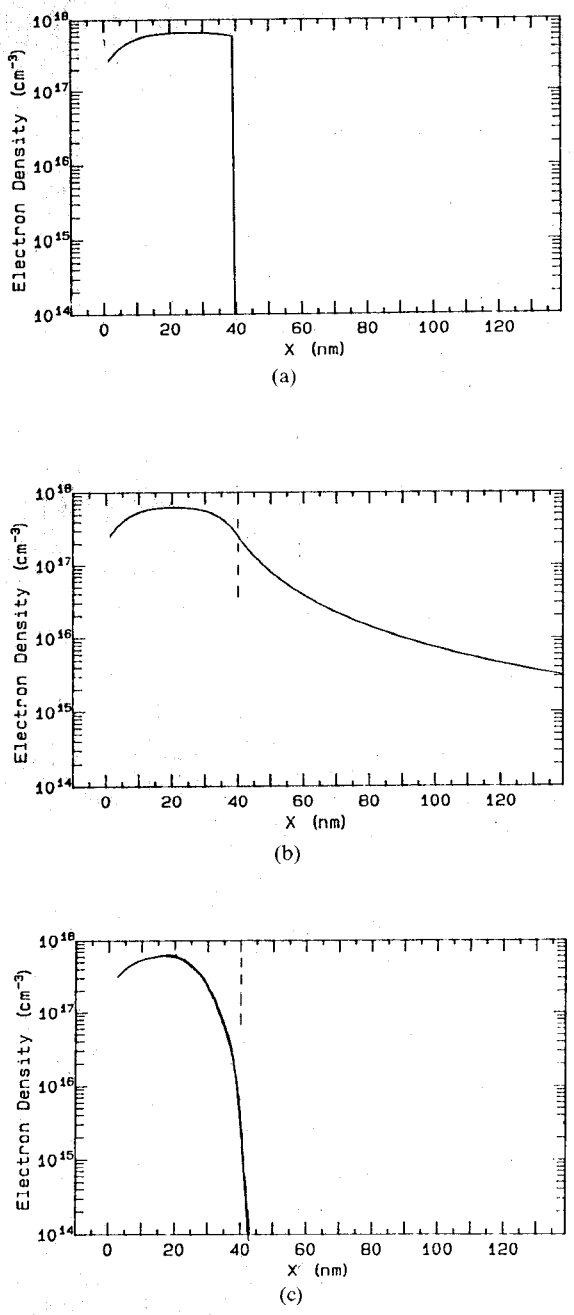


Fig. 5. Electron charge distribution in various MESFET active layers. (a) MESFET with AlGaAs buffer. (b) Standard MESFET. (c) MESFET with p^+ barrier layer.

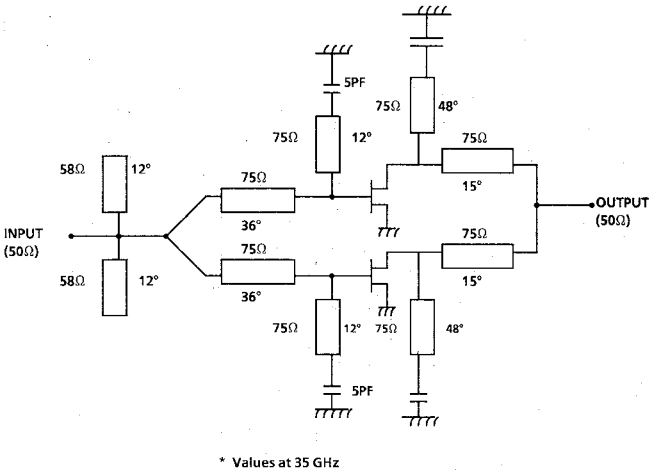


Fig. 6. Circuit topology of a monolithically matched 400 μm FET at 35 GHz.

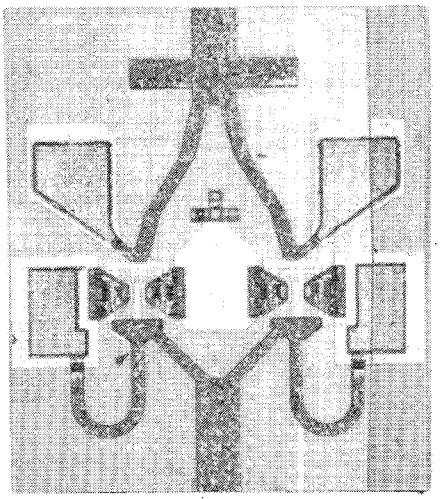


Fig. 7. A SEM photograph of a completed amplifier (2×200 μm^2 FET).

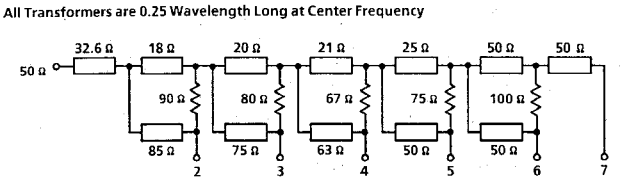


Fig. 8. Schematic of six-way power divider/combiner.

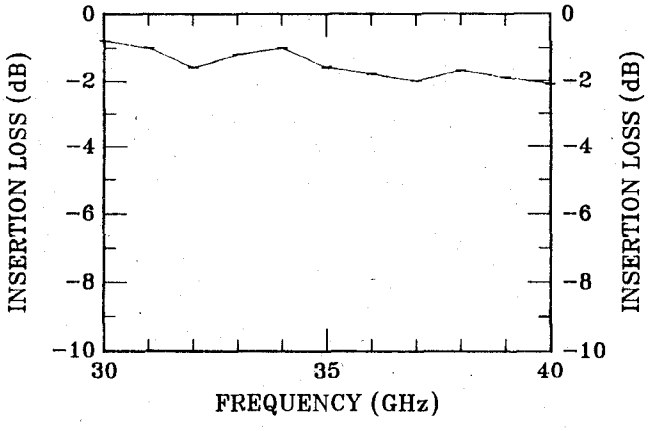
On the average, the amplifiers produced 126 mW of output power with 5 dB gain [11].

IV. Six-Way Power-Combined Amplifier

With the increased interest in a high output power amplifier at *Ka*-band, there is a need for a broad-band power-combining scheme that can alleviate the device size and impedance level limitations. The traveling-wave divider/combiner approach [16], [17] is very attractive for monolithic implementation because of its planar structure and inherent broad-band interport isolation characteristics. This is especially true for millimeter-wave frequencies, where, due to the reduced wavelength, the transformer lengths become reasonable for a compact design. Fig. 8 shows the schematic diagram of a six-way traveling-wave power combiner. All the transformers are 0.25 wavelength long at 35 GHz. It is seen that all the characteristic impedances of the transformers can be realized on 100-μm-thick GaAs substrates.

Fabrication of the divider/combiner is quite simple and completely compatible with the GaAs FET fabrication process. There are only three mask levels: resistors, conductor metal, and gold plating (to increase conductivity). Fig. 9 is a photo of the completed divider/combiner, along with its RF insertion loss curve. As shown, the six-way

(a)



(b)

Fig. 9. The six-way divider/combiner. (a) Photo of the device. (b) Insertion loss.

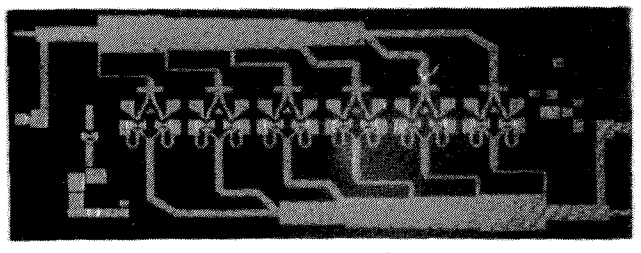


Fig. 10. Photo of six-way power-combined monolithic amplifier chip.

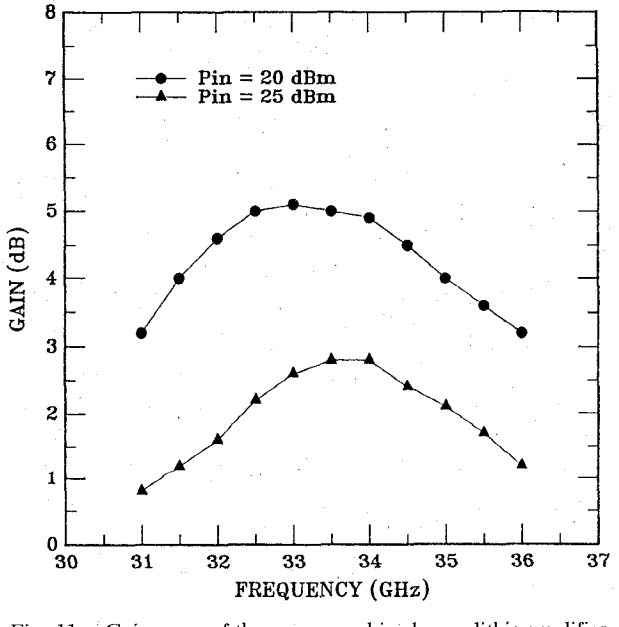


Fig. 11. Gain curve of the power-combined monolithic amplifier.

divider/combiner, designed at the center frequency of 35 GHz, has a propagation loss in back-to-back connection of 1 to 2 dB across the 30 to 40 GHz band. This implies about 1 dB loss in the divider and 1 dB in the combiner.

The 400 μm amplifiers were monolithically power-combined using the integrated divider/combiner on a single chip. Fig. 10 shows the processed monolithic chip, $105 \times 285 \times 4$ mils in size. The 0.25-μm-gate FET amplifiers were processed on a standard doped active layer. Fig. 11 shows the performance of the amplifier. With an input power of 100 mW, the gain was 5.2 dB centered at 33 GHz. The amplifier generated 0.5 W of output power with 4 dB gain and 0.6 W with 2.8 dB gain [11]. The power output was limited by the low gain of the amplifier. The output was compressed less than 1 dB even at 0.6 W output power. Further improvements in output power are expected using two-stage amplifiers as a unit cell. Even further improvements are expected using the optimized power MESFET's discussed above.

V. Conclusions

We have investigated the power MESFET structure. The best power output density has been achieved using a MESFET on AlGaAs buffer. The best combination of high output power density and power-added efficiency has been obtained using a MESFET on a very heavily doped active layer. At 35 GHz, an output power density of 0.71 W/mm has been achieved with 5.2 dB gain and 34 percent efficiency. When tuned for maximum efficiency, the MESFET's had a 41 percent power-added efficiency at a power density of 0.61 W/mm with 5.6 dB gain. These results show that GaAs MESFET's can perform as well as devices with more complex heterostructures, such as HEMT's or pseudomorphic HEMT's at *Ka*-band [18].

Monolithic amplifiers have been developed. For large output power, six 400 μm FET amplifiers were monolithically integrated, and the resulting device delivered 0.6 W output power with 2.8 dB gain. The amplifier was built using nonoptimized power MESFET's. With further effort, a monolithic power amplifier with 1 W at *Ka*-band will be possible.

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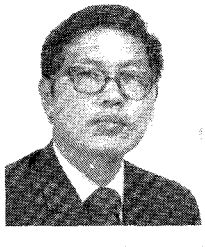

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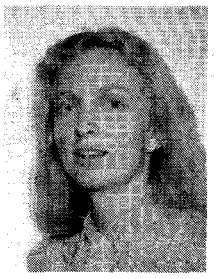

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Ms. Wurtele is the coauthor of several technical papers.